SYSTEM AND METHOD FOR DISCONNECTING A PORTION OF AN INTEGRATED CIRCUIT

Field of the Invention

The present invention relates the field of integrated circuit (IC) design. More particularly, it relates to a system and method for disconnecting or isolating a designated portion of an integrated circuit, either permanently or temporarily.

BACKGROUND OF THE INVENTION

As integration levels of integrated circuits expand, semiconductor chip size has continuously increased, and accordingly, each chip may contain a plurality of macros. These macros may be of similar functionality, such as memory arrays (i.e., DRAMs), or of differing functionality, such as mixed digital and analog macros. The production yield of these chips can be greatly improved if extra, or redundant, macros are prepared.

An article entitled "256-Mb DRAM Circuit Technologies for File Applications" in the IEEE Journal of Solid State Circuits, vol. 28, no. 11, November 1993, pp. 1105-1113, discusses the effect that chip integration has had on chip yield. FIG. 1 is a chart taken from the article showing the ratio of these different faults for each generation of DRAM technology. As shown in FIG. 1, the trend indicates as the integration level has progressed,

the fatal fault and excessive stand-by current fault (Isb fault) over-dominates the traditional bit and line fault.

To improve chip yield, several redundancy schemes have been employed to overcome the Isb fault. One such scheme is to remove a power supply to a defective macro on the chip. For example, one can design a power switch for each macro, so when the macro is found to be defective, the power switch is turned off and the supply power to the macro is cut-off. However, this scheme requires a large area of the integrated circuit chip to form a low impedance switch. Additionally, when the switch is large, it is vulnerable and subject to off-state leakage. On the other hand, if the switch is not properly sized, the impedance could hurt the circuit performance.

The above-mentioned article suggests a sub-array replacement redundancy scheme, as shown in FIG. 2, employing a power switch and fuse ROM. In this scheme, all sub-arrays of a macro are tested one by one concerning DC current. The fuse ROMs are used to store the test results and control the switches. The power switches of the defective sub-arrays are turned off and the power switches for the good spare sub-arrays are turned on.

Another well-known prior art scheme is to use "header" and "footer" devices to selectively switch on and off a portion of a circuit, i.e., a defective macro. Similar to the power switch scheme, this approach is not area efficient. Besides, it consumes energy to switch on and off the huge header and footer devices.

Another approach is to provide an array of laser, or electrical, fuses between an external power supply and the macro power supply system. An array of fuses is needed in order to avoid high impedance occurrences in the power supply. When a macro must be disabled, the whole array of fuses is blown using conventional blowing techniques. Due to the ablative nature of fuse blowing techniques, this scheme is not a clean process. For example, sometimes, the remaining debris could form an unwanted high resistive path, especially when blowing a full array of fuses located in close proximity to each other. Unlike signal fuse blowing, this scheme is not a fully reliable method. Besides, this is a non-reversible process, once the macro is blown, it cannot be reconnected to the power supply.

SUMMARY

Accordingly, it is an aspect of the present invention to provide a system and method for selectively disconnecting a designated portion of an integrated circuit, either permanently or temporarily, without affecting normal operation of the integrated circuit.

Another aspect of the present invention is to provide a DC voltage generator system for disconnecting a designated portion of an integrated circuit.

It is a further aspect of the present invention to provide a DC voltage generator system for disconnecting a defective macro of an integrated circuit to eliminate cross-macro noise coupling and voltage leakage.

Finally, another aspect of the present invention is to provide a DC voltage generator system for disconnecting a designated portion of an integrated circuit where the designated portion is capable of being reconnected at a later time due to a need in increased capacity or to replace other failed portions.

Accordingly, the present invention provides an integrated circuit system having a plurality of macros. The integrated circuit system includes an external voltage supply input configured for supplying an external voltage to the integrated circuit; and a plurality of internal voltage supply generators, each of the plurality of internal voltage supply generators being connected to a respective macro of the plurality of macros and configured for receiving the external voltage via the external voltage supply input for generating an internal voltage supply for operating its respective macro. Each of the plurality of internal voltage supply generators includes circuitry for generating the internal voltage supply and circuitry for disconnecting at least a portion of its respective macro. The integrated circuit system can be applied to a semiconductor chip to save active or stand-by power. It can also be used to disconnect a defective portion of the chip and optionally replace it with a non-defective portion of the chip.

According to the integrated circuit system of the present invention, any unwanted portion(s) of the integrated circuit system (i.e., a grossly defective macro, a macro with excessive stand-by current due to local power short, and/or an unnecessary macro based on

the current application) which can not be fixed by the on-chip redundancy elements are made detachable from the rest of the system. For example, during testing, if a macro is found to have a high level of DC leakage, the whole macro is disconnected from the rest integrated circuit system by removing the power supply to that macro so that the leakage problem due to any cause can be eliminated. Thereafter, once the defective macro is disconnected, one of a predetermined number of extra macros can be enabled so the remaining memory capacity can still meet customer's specifications.

The integrated circuit system of the present invention, which will be described below in detail, has many advantages: (1) the internal power supply is regulated; (2) any macro or sub-macro can be disconnected from the power supply temporarily or permanently, whether they are defective or not for power saving purposes; (3) any macro or sub-macro can be reconnected back to the power supply, if more macros are needed for different applications for flexibility; (4) the system is fully compatible with an ASIC (Application Specific Integrated Circuit) environment, that is during power-on, the unwanted or defective macros can be programmed to be shut-off by scanning a disable command into each macro; (5) each macro can be sequentially or parallelly tested during a test mode, thus saving test cost; (6) cross-macro noise coupling is eliminated, since the power supply to each macro is isolated from the rest of the macros; and (7) the DC voltage

leakage associated with an off-state DC voltage generator is much lower than the prior art power switch scheme.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a chart illustrating yield improvement of DRAM chips through redundancy techniques;

FIG. 2 is a prior art schematic diagram of a sub-array replacement redundancy scheme;

FIG. 3 is a block diagram of an integrated circuit system in accordance with the present invention having eight identical macros;

FIG. 4 is a block diagram of an internal voltage supply generator of the integrated circuit system in accordance with the present invention; and

FIG. 5 is a detailed block diagram of the internal voltage supply generator of FIG 4.

DETAILED DESCRIPTION OF THE INVENTION

With reference to FIG. 3, there is shown an integrated circuit system 100 for selectively disconnecting or isolating a designated portion of the system in accordance with the present invention. By way of example, FIG. 3 illustrates an exemplary integrated circuit chip system comprising eight identical macros A1-A8, in which each macro is preferably an

independently executable embedded DRAM. Based on the maturity of the design and technology stage, it will be assumed that two extra macros are sufficient for replacing up to two defective macros.

The integrated circuit system 100 of the present invention includes an external power supply Vext 170 and a global ground Gnd 160 which are connected to each macro A1-A8 via a set of properly sized power bus lines. Each macro A1-A8 is equipped with its own internal voltage supply generator 130 (Vint Gen). This internal voltage supply generator 130 receives an external power supply and generates an internal power supply. In a preferred embodiment, the external power supply level is greater than the internal power supply level.

The internal voltage supply generator 130 also provides a voltage supply to generate other voltage levels, such as the boosted wordline high level Vpp, the negative word line level Vwl, and the substrate bias level Vbb, etc. (see FIG. 4). The generated and regulated Vint power supply network 110 of each macro A1-A8 is isolated from each other, therefore, cross-macro noise coupling can be minimized. The Vint power supply network 110 provides the generated internal power supply level, e.g., a voltage supply, to individual circuits and/or components, such as sense amplifier circuits, row and column decoders, etc., within each macro A1-A8 during operation.

The internal voltage supply generator 130 not only generates the internal power

supply level, but also regulates the internal power supply level. As chips grow bigger, the internal power regulation of the internal voltage supply generator 130 becomes very critical in order to guarantee circuit performance. Such a local regulation will avoid any detrimental consequence caused by supply voltage instability either due to RC drop or noise effects.

Within each internal voltage supply generator 130, there is a switching mechanism which can switch the generator 130 on and off. This switching mechanism and the related DC system components within each macro A1-A8 will be discussed below with reference to FIG. 5. To control the switching mechanism, a scan-chain 150 formed by a chain of scannable enable registers 140 is provided. During a power-up period for the chip, fuse information, which determines row and column redundancy replacement, and a switch enable/disable signal, i.e., a logic high or logic low value, are scanned and stored in the corresponding latches 140 of each macro A1-A8. When power-up is over, the chip is ready for a normal operation and, for those macros A1-A8 which are disabled by the system, i.e., for example, a logic low enable signal is stored within their corresponding latch 140, their internal voltage supply generator 130 is disabled, and therefore, no power is generated to these macros A1-A8. Accordingly, these macros A1-A8 will be isolated, or disconnected, from the rest of the macros A1-A8.

An exemplary internal voltage supply generator 130 for each macro A1-A8 is

shown in FIG. 4. First, the external power supply Vext 170 generates a reference voltage level, e.g. a DC reference or band-gap reference, through reference voltage generator 180. These reference voltage levels are used to first generate an internal voltage supply Vint via Vint generator 182. Depending on the layout and power demand, a plurality of Vint generators 182 may be provided. Through the generated internal voltage supply Vint and reference voltage Vref, many other voltage levels, such as the substrate bias level Vbb, the negative word line level Vwl, and the boosted wordline high level Vpp are generated via the respective generators Vbb Gen 184, Vwl Gen 186, and Vpp Gen 188. Therefore, when the Vint generator 182 is switched off, the rest of the generators 184, 186, 188 will also stop functioning, and the power supply to the respective macro A1-A8 will be completely off.

A more detailed block diagram of the internal voltage supply generator 130 is shown in FIG. 5. The internal voltage supply generator 130 includes a voltage and/or current reference supply unit 210 which can be identical to the voltage reference generator 180. The reference levels of reference supply unit 210 can be produced from a bandgap reference whose value is independent of temperature, process, and power supply level as is known in the art. The reference levels can also be a voltage and/or temperature dependent voltage or current reference level depending on the design requirements. The internal voltage supply generator 130 further includes voltage limiter 220, an oscillator 230, a charge pump 240 having at least one reservoir capacitor (not shown) and the enable register

140.

The voltage and current reference levels are fed into the voltage limiter 220 to control an output voltage level. The voltage limiter 220 includes a voltage divider and a differential amplifier, as is known in the art, for limiting or controlling the voltage or current reference levels generated by the reference supply unit 210. Based on the feedback voltage level of Vint and the reference voltage level, the differential amplifier determines whether the oscillator 230 and the charge pump 240 should be turned on or off.

Once the oscillator 230 is turned on, it generates an oscillating voltage level for pumping or driving the charge pump circuit 240 to generate the internal voltage supply level Vint. Note that all the components 210, 220, 230, 240 and 140 are powered by the external power supply Vext 170.

During power-up, the information that is scanned and stored in the enable register 140 determines whether the internal voltage supply generator 130 should be disabled or not. If a low state signal (disable signal) is stored in the register 140, then it automatically switches off the voltage limiter 220, the oscillator 230, and the charge pump 240 by transmitting a disable signal via control lines A, B and C, respectively, which form the switching mechanism discussed above.

At this point, the Vint generator 130 is completely turned off, and there is no floating state within these circuits. Accordingly, the Vint generator 130 is disconnected or

isolated from the external voltage supply. On the other hand, if a high state signal (enable signal) is stored in register 140, the voltage limiter 220, the oscillator 230, and the charge pump 240 are activated by an enable signal via control lines A, B and C and an internal power supply is provided to the corresponding macro A1-A8.

Once the internal voltage supply generator 130 is turned off, the leakage of the external power supply Vext 170 through the DC components are much lower than that of conventional power switches. This is due to the fact that the total device size for the voltage limiter 220, the oscillator 230, and the charge pump 240 is much smaller than that of a power switch. Typically, in order to avoid power loss due to a power switch, the switch is made large or is a wide channel device. Consequently, the wider the channel width, the higher the subthreshold current and subsequent leakage.

The integrated circuit system 100 of the present invention can disconnect any macro from the rest of the system for at least two reasons: (1) the macros are known to be defective. The defective macro addresses are recorded in a fuse bank 120 (see FIG. 3), and the fuse information is used to disable these macros, so that during normal operation theses macros are isolated or disconnected from the integrated circuit system; and (2) in order to save power. For example, during a low-power mode, less than the total number of macros may be needed to store only mission critical information. When less than the total number of macros is used, chip power consumption can be significantly reduced.

Another feature of this design is the hierarchical built-in self test (BIST) concept. With reference to FIG. 1, a central BIST circuit block 160 is provided, as known in the art, to handle BIST operation at a global level. That is, the central BIST 160 communicates with local BIST residing in each macro A1-A8 for controlling, testing and supervising purposes. The central BIST circuit block 160 controls the execution of the testing operations for all the local BIST circuits. In a normal operation, it controls the global fuse scanning by providing a scan clock and a control signal during the power-on period.

The concept of the present invention can be extended to be able to disconnect individual circuit components and/or circuits within the macros A1-A8 based on discovered faults or other reasons. For example, a DC voltage generator of a particular sub-array within a macro can be turned off, if, for example, that sub-array is found to have excessive stand-by current.

The sub-array within the macro can be turned off by cutting off a supply voltage from reaching the sub-array by providing one or more switches within the Vint power supply network 110 to regulate which components/circuits receive a voltage supply within the macro. The sub-array within the macro can then be fixed or replaced. Additionally, all of the DC generators within a particular macro can be turned off if there is a fatal fault within that macro to completely disconnect the macro from the other macros.

What has been described herein is merely illustrative of the application of the principles of the present invention. For example, the functions described above and implemented as the best mode for operating the present invention are for illustration purposes only. Other arrangements and methods may be implemented by those skilled in the art without departing from the scope and spirit of this invention.